What is claimed is:

1. A four-transistor random access memory cell comprising:

a first transistor of a first conductivity type having a gate coupled to a word line and a source coupled to a bit line;

a second transistor of the first conductivity type having a gate coupled to a drain of the first transistor and a source coupled to receive a first voltage;

a third transistor of a second conductivity type having a gate coupled to a drain of the second transistor, a source coupled to receive a second voltage and a drain coupled to the drain of the first transistor; and

a fourth transistor of the second conductivity type having a gate coupled to the drain of the first transistor, a source coupled to receive the second voltage and a drain coupled to the drain of the second transistor.

2. The four-transistor random access memory cell as in claim 1, wherein the first transistor further comprises a bulk coupled to receive a third voltage.

3. The four-transistor random access memory cell as in claim 2, wherein the first voltage is V_{dd}, the second voltage is a ground voltage and the third voltage is V_{PP} higher than V_{dd}.

4. The four-transistor random access memory cell as in claim 2, wherein the first voltage is V_{dd}, the second voltage is V_{bb} and the third voltage is V_{PP} higher than V_{dd}.

5. The four-transistor random access memory cell as in claim 1, wherein the second transistor further comprises a bulk coupled to receive a third voltage.

6. The four-transistor random access memory cell as in claim 5, wherein the first voltage is V_{dd}, the second voltage is a ground voltage and the third voltage is V_{PP} higher than V_{dd}.

7. The four-transistor random access memory cell as in claim 5, wherein the first voltage is V_{dd}, the second voltage is V_{bb} and the third voltage is V_{PP} higher than V_{dd}.

8. The four-transistor random access memory cell as in claim 1, wherein the first transistor further comprises a bulk coupled to receive the first voltage.

9. The four-transistor random access memory cell as in claim 8, wherein the first voltage is V_{dd} and the second voltage is a ground voltage.

10. The four-transistor random access memory cell as in claim 8, wherein the first voltage is V_{dd} and the second voltage is V_{bb}.

11 The four-transistor random access memory cell as in claim 1, wherein the second transistor further comprises a bulk coupled to receive the first voltage.

12. The four-transistor random access memory cell as in claim 11, wherein the first voltage is V_{dd} and the second voltage is a ground voltage.

13. The four-transistor random access memory cell as in claim 11, wherein the first voltage is V_{dd} and the second voltage is V_{bb}.

14. The four-transistor random access memory cell as in claim 1, wherein the first and second conductivity types are respectively P and N type.

15. A random access memory cell comprising:
a first transistor of a first conductivity type having a gate coupled to a word line and a source coupled to a bit line;
a second transistor of a second conductivity type having a source coupled to receive a second voltage and a drain coupled to the drain of the first transistor;
a diode having an anode coupled to the drain of the first transistor and a cathode coupled to receive a first voltage; and
an inverter having an input terminal coupled to the drain of the first transistor and an output terminal coupled to a gate of the second transistor.

16. The random access memory cell as in claim 15, wherein the inverter comprises:

a third transistor of the first conductivity type having a gate coupled to the drain of the first transistor and a source coupled to receive the first voltage; and

a fourth transistor of the second conductivity type having a gate coupled to the drain of the first transistor, a source coupled to receive the second voltage and a drain coupled to the drain of the third transistor.

17. The random access memory cell as in claim 16, wherein the first and third transistor each comprise a bulk coupled to receive a third voltage.

18. The random access memory cell as in claim 17, wherein the first voltage is V_{dd}, the second voltage is a ground voltage and the third voltage is V_{PP} higher than V_{dd}.

19. The random access memory cell as in claim 17, wherein the first voltage is V_{dd}, the second voltage is V_{bb} and the third voltage is V_{PP} higher than V_{dd}.

20. The random access memory cell as in claim 16, wherein each of the first and third transistors comprises a bulk coupled to receive the first voltage.

21. The random access memory cell as in claim 20, wherein the first voltage is V_{dd} and the second voltage is a ground voltage.

22. The random access memory cell as in claim 20, wherein the first voltage is V_{dd} and the second voltage is V_{bb}.

23. The random access memory cell as in claim 16, wherein the diode is formed by a junction between the bulk and drain of the first transistor.

24. A memory device comprising:

a plurality of memory cells wherein data is read from and written into each of the memory cells through bit lines by control signals on word lines, each of the memory cells comprising:

a first transistor of a first conductivity type having a gate coupled to one of the word lines and a source coupled to one of the bit lines;

a second transistor of the first conductivity type having a gate coupled to a drain of the first transistor and a source coupled to receive a first voltage;

a third transistor of a second conductivity type having a gate coupled to a drain of the second transistor, a source coupled to receive a second voltage and a drain coupled to the drain of the first transistor; and

a fourth transistor of the second conductivity type having a gate coupled to the drain of the first transistor, a source coupled to receive the second voltage and a drain

coupled to the drain of the second transistor.

25. The memory device as in claim 24, wherein the first transistor further comprises a bulk coupled to receive a third voltage.

26. The memory device as in claim 25, wherein the first voltage is V_{dd}, the second voltage is a ground voltage and the third voltage is V_{PP} higher than V_{dd}.

27. The memory device as in claim 25, wherein the first voltage is V_{dd}, the second voltage is V_{bb} and the third voltage is V_{PP} higher than V_{dd}.

28. The memory device as in claim 24, wherein the second transistor further comprises a bulk coupled to receive the third voltage.

29. The memory device as in claim 28, wherein the first voltage is V_{dd}, the second voltage is a ground voltage and the third voltage is V_{PP} higher than V_{dd}.

30. The memory device as in claim 28, wherein the first voltage is V_{dd}, the second voltage is V_{bb} and the third voltage is V_{PP} higher than V_{dd}.

31. The memory device as in claim 24, wherein the first transistor further comprises a bulk coupled to receive the first voltage.

32. The memory device as in claim 31, wherein the first voltage is V_{dd}, the second voltage is a ground voltage and the third voltage is V_{PP} higher than V_{dd}.

33. The memory device as in claim 31, wherein the first voltage is V_{dd}, the second voltage is V_{bb} and the third voltage is V_{PP} higher than V_{dd}.

34. The memory device as in claim 24, wherein and the second transistor further comprises a bulk coupled to receive the first voltage.

35. The memory device as in claim 34, wherein the first voltage is V_{dd}, the second voltage is a ground voltage and the third voltage is V_{PP} higher than V_{dd}.

36. The memory device as in claim 34, wherein the first voltage is V_{dd}, the second voltage is V_{bb} and the third voltage is V_{PP} higher than V_{dd}.

37. The memory device as in claim 24, wherein the first and second conductivity types are P and N type respectively.

38. A memory device comprising:

a plurality of memory cells wherein data is read from and written into each of the memory cells through bit lines by control signals on word lines, each of the memory cells comprising:

a first transistor of a first conductivity type having a gate coupled to a word line and a source coupled to a bit line;

a second transistor of a second conductivity type having a source coupled to receive a second voltage and a drain coupled to the drain of the first transistor;

a diode having an anode coupled to the drain of the first transistor and a cathode coupled to receive a first voltage; and

an inverter having an input terminal coupled to the drain of the first transistor and an output terminal coupled to a gate of the second transistor.

39. The memory device as in claim 38, wherein the inverter further comprises:

a third transistor of the first conductivity type having a gate coupled to the drain of the first transistor and a source coupled to receive the first voltage; and

a fourth transistor of the second conductivity type having a gate coupled to the drain of the first transistor, a source coupled to receive the second voltage and a drain coupled to the drain of the third transistor.

40. The memory device as in claim 39, wherein the first and third transistors each comprise a bulk coupled to receive a third voltage.

41. The memory device as in claim 40, wherein the first voltage is Vdd, the second voltage is a ground voltage and the third voltage is VPP higher than Vdd.

42. The memory device as in claim 40, wherein the first voltage is Vdd, the second voltage is V_{bb} and the third voltage is VPP higher than Vdd.

43. The memory device as in claim 39, wherein the first and third transistors each comprise a bulk coupled to receive the first voltage.

44. The memory device as in claim 43, wherein the first voltage is Vdd and the second voltage is a ground voltage.

45. The memory device as in claim 39, wherein the diode is formed by a junction between the bulk and drain of the first transistor.

46. A 4T-SRAM cell in a SRAM array having pairs of a first and second bit line, and a first and second word line, comprising:

a first transistor of a first conductivity type having a gate coupled to one of the first word lines and a source coupled to one of the first bit lines;

a second transistor of the first conductivity type having a gate coupled to a drain of the first transistor and a source coupled to receive a first voltage;

a third transistor of a second conductivity type having a gate coupled to a drain of the second transistor, a source coupled to receive a second voltage and a drain coupled to the drain of the first transistor; and

a fourth transistor of the second conductivity type having a gate coupled to one of the second word lines, a source coupled to one of the second bit lines and a drain coupled to the gate of the third transistor.

47. The 4T-SRAM cell as in claim 46, wherein bulks of the first and fourth transistor are respectively coupled to receive the first and second voltage.

48. The 4T-SRAM cell as in claim 46, wherein the first and second conductivity types are respectively P and N type.